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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known			
		Application Number	10/023,435		
		Filing Date	December 14, 2001		
		First Named Inventor	WU, Yu-Liang		
		Art Unit	2825		
		Examiner Name	Liu		
Sheet	1	of	3	Attorney Docket Number	TAH-001.00

U.S. PATENT DOCUMENTS					
Examiner Initials ⁷	Cite No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
AS		US-4,593,363 A	06-03-1986	BURSTEIN et al.	
AS		US-5,396,435 A	03-07-1995	GINETTI	
AS		US-5,596,743 A	01-21-1997	BHAT et al.	
AS		US-6,282,695 B1	08-28-2001	REDDY et al.	
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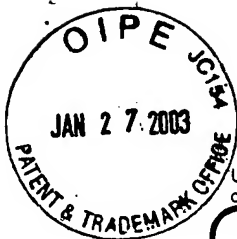
FOREIGN PATENT DOCUMENTS						
Examiner Initials ⁷	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶

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APPLICANT-MODIFIED PTO/SB/08B (10-01)

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		Examiner Name	LIU
Sheet 2 of 3	Attorney Docket Number	TAH-001.00	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
AZ		W. KUNZ, and D.K. PRADHAN; "Recursive Learning: A New Implication Technique for Efficient Solutions to CAD Problems--Test, Verification, and Optimization"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Sep. 1994; pp. 1143-1158; Vol. 13, No. 9.	
AZ		L.A. ENTRENA and K.T. CHENG; "Combinational and Sequential Logic Optimization by Redundancy Addition and Removal"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Jul., 1995; pp. 909-916.	
AZ		L.A. ENTRENA, J.A. ESPEJO, E.OLIAS, and J. UCEDA; "Timing Optimization by an Improved Redundancy Addition"; Proc., European Design Automation Conf. 1996; Sep., 1996; pp. 342-347; Geneva, Switzerland.	
AZ		S.C. CHANG, L.P.P.P. VAN GINNEKEN, and M. MAREK-SADOWSKA; "Fast Boolean Optimization by Rewiring", Proc., IEEE/ACM Int. Conf. on Computer-Aided Design 1996; Nov., 1996; pp. 262-269; San Jose, U.S.A.	
AZ		S.C. CHANG, M. MAREK-SADOWSKA, and K.T. CHENG; "Perturb and Simplify: Multilevel Boolean Network Optimizer", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Dec., 1996; pp. 1494-1504; Vol. 15, No. 12.	
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AZ		S.C. CHANG, L.P.P.P. VAN GINNEKEN, M. MAREK-SADOWSKA; "Circuit Optimization by Rewiring", IEEE Transactions on Computers; Sep., 1999; pp. 962-970; Vol. 48, No. 9.	
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AZ		Y.L. WU, W. LONG, and H. FAN. "A Fast Graph-Based Alternative Wiring Scheme for Boolean Networks"; Proc., IEEE 13th Int. Conf. on VLSI Design 2000; Jan., 2000; pp. 268-273; India.	

Examiner Signature		Date Considered	5/30/03
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AJ		Y.L. WU, W. LONG, and H.B. FAN; "A Fast Graph-Based Alternative Wiring Scheme for Boolean Networks"; IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences; June 2000; pp. 1131-1137; Vol. E83-A, No.6.	
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AJ		C.W. CHANG, and M. MAREK-SADOWSKA; "Who Are the Alternative Wires in Your Neighborhood? (Alternative Wires Identification Without Search)"; Proc., Great Lakes symposium on VLSI 2001; Mar., 2001; pp. 103-108; West Lafayette, U.S.A.	
AJ		C.W. CHANG, and M. MAREK-SADOWSKA; "Single-Pass Redundancy and Removal"; Proc., Int. Conf. on Computer-Aided Design 2001; Nov., 2001; pp. 606-609. San Jose, U.S.A.	

Examiner Signature	<i>Andrew L.</i>	Date Considered	5/30/03
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